Amendments to the Claims

Claim 1 (currently amended): ~~A single layer of insulating material~~ An interlevel dielectric directly contacting and formed between ~~conductive elements~~ successive metallization levels in an integrated circuit, without other intervening materials between the successive metallization levels, the interlevel dielectric comprising a polysiloxane network consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon-silicon bonding and having a dielectric constant of less than about 3.3.

Claim 2 (currently amended): The ~~insulating material~~ interlevel dielectric of Claim 1, having a dielectric constant of less than about 3.2.

Claim 3 (currently amended): The ~~insulating material~~ interlevel dielectric of Claim 1, having a carbon content of between about 5% and 20% relative to a silicon content.

Claim 4 (currently amended): The ~~insulating material~~ interlevel dielectric of Claim 1, wherein the ~~conductive elements~~ successive metallization levels comprise metal runners.

Claim 5 (currently amended): An integrated circuit having an electrical path, the integrated circuit comprising:

a first ~~conductive element~~ metallization level providing a first portion of the electrical path ~~of the circuit~~;

a second ~~conductive element~~ metallization level providing a second portion of the electrical path ~~of the circuit~~, the second ~~conductive element~~ metallization level separated from the first ~~conductive element~~ metallization level by a gap; and

~~a single insulating layer~~ an interlevel dielectric directly contacting the first and second ~~conductive elements~~ metallization levels and filling the gap between the first and second metallization levels ~~conductive elements~~, the ~~insulating layer~~

interlevel dielectric comprising polysiloxane, consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon therein and having a dielectric constant of less than about 3.5.

Claim 6 (currently amended): The integrated circuit of Claim 5, wherein the ~~insulating layer~~ interlevel dielectric has a dielectric constant of less than about 3.3.

Claim 7 (currently amended): The integrated circuit of Claim 6, wherein the first and second ~~conductive elements~~ metallization levels are metal runners.

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Claim 8 (currently amended): The integrated circuit of Claim 6, wherein the first and second ~~conductive elements~~ metallization levels are transistor active areas within a semiconductor substrate.

Claim 9 (currently amended): The integrated circuit of Claim 8, wherein the ~~insulating layer~~ interlevel dielectric comprises a sidewall spacer.

Claim 10 (currently amended): The integrated circuit of Claim 9, wherein the first ~~conductive element~~ metallization level is a transistor gate electrode and the second ~~conductive element~~ metallization level is a contact to a transistor active area.